REMARKS

The claims are claims 5, 7, 10, 11, 12, 16, 17, 19, 20, 21 and 22.

Claims 5, 10, 11, 12, 16, 17, 19 and 20 are amended. Claims 1, 2, 3, 4, 6, 8, 9, 13, 14, 15, 19 and 21 are canceled. Claims 5, 10, 11, 12, 16, 17, 19 and 20 are amended to incorporate the limitations of canceled base claim 1.

Claims 10 and 11 are rejected under 35 U.S.C. 102(b) as anticipated by White U.S. Patent No. 5,689,693. The OFFICE ACTION cites the same parts of White at column 6, line 65 to column 7, line 31 and column 9, lines 49 to 62 as anticipating these claims.

Claim 10 recites subject matter not anticipated by White. Claim 10 recites "wherein the annul code is generated in response to one or more constant generating instructions and loaded into the annul word memory." White states at column 6, line 65 to column 7, line 31:

> "Referring to FIG. 2, reorder buffer 126 includes a reorder buffer (ROB) control and status block 270, a reorder buffer (ROB) array 274, and a reorder buffer (ROB) operand bus driver 276. ROB control and status block 270 is connected to the A and B-operand pointers 136 and 137 and the destination pointer busses 143 to receive inputs which identify source and destination operands for an ROP. ROB array 270 is connected to the result busses 132 to receive results from the functional units. Control signals, including a head pointer 216, a tail pointer 218, an A operand select 222, a B operand select 224 and a result select 226, are conveyed from ROB control and status 270 to ROB array 274. These control signals select ROB array elements that are written with result busses 132 data and read to writeback busses 134, write pointers 133, A and B-operand busses 130 and 131, and A and B-operand tag busses 148 and 149. Sixteen destination pointers 220 (DEST PTRS), one for each reorder buffer array element, are conveyed from ROB array 274 to ROB control and status 270 to check for data dependencies.

"ROB array 274 is a memory array under the control of the ROB control and status block 270. As the instruction decoder 118 dispatches ROPs, it places pointers on the four destination pointer busses 143. ROB control status 270 then allocates an entry of ROB array 274 and writes the destination register pointer into the DEST PTR field of the allocated entry.

"As operations are executed and results are placed on the result busses 132 by the functional units, ROB control and status 270 accesses pointers from the result tag busses 132 which designate the corresponding ROB array entries to receive data from the result busses 132. ROB control 270 directs writing from the result busses 132 to the ROB array 274 using five result select pointers 226."

This portion of White fails to include description of any instruction. This portion of White likewise fails to recite any generation of a constant. White states at column 9, lines 49 to 62:

"In addition, the reorder buffer 126 handles data resulting from speculative ROP execution. For successfully predicted branches, the reorder buffer 126 entry allocated to the branch ROP holds the branch target program counter. For mispredicted branches, the reorder buffer 126 entry allocated to the branch ROP stores an indicator that the branch ROP is mispredicted. All speculative reorder buffer entries following a mispredicted branch are invalid. The reorder buffer records this invalidity by setting a "cancel" bit in the reorder buffer array 274 status and control field <23:0> for each of the invalid entries. When the invalid entries are retired, their results are discarded and processor resources, such as the register file 124, are not updated. The reservation stations of the functional units are not flushed."

This portion of White fails to include description of any instruction. This portion of White likewise fails to recite any generation of a constant. In the absence of any teaching of any of the relevant limitations of claim 10, White fails to anticipate claim 10.

Claim 11 recites subject matter not anticipated by White. Claim 11 recites "wherein the annul code is loaded into the annul word memory from a memory." The cited portions of White are quoted above. These portions of White fail to provide any teaching that he annul code is loaded from a memory. In the absence of any teaching of any of the relevant limitation of claim 11, White fails to anticipate claim 11.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

Robert D. Marshall, Jr.
Reg. No. 28,527